IN THE CLAIMS:

1. (Previously Presented) A serializer for sending a data word out bit by bit, the serializer comprising:

a register for holding the data word, the register having at least one data output and a control input;

an output data port for serially outputting the data word bit by bit;

means for connecting the data output to the output data port;

a pulse generator free of external timing reference;

means for connecting the pulse generator to the control input after a data word has been loaded into the register, wherein the data word bits are serially output in response to the pulse generator; and

means for adding at least two boundary bits to the serially output data word bits, wherein the added two bits always include a logic one and a logic zero in any order, and further wherein the means for connecting the pulse generator to the control input includes means for holding the signal at the control input at a constant logic level during the outputting of the at least two added bits.

2. (Previously Presented) The serializer of claim 1 further comprising means for outputting a data word boundary for separating data words, the data word boundary comprised of a combination of pulse generator signals and the at least two signals added to the serially output data word bits.

3. (Canceled)

4. (Original) The serializer of claim 1 wherein the register is a shift register.

5. (Original) The serializer of claim 1 further comprising a multiplexer arranged to select the at least one register output and connect it to the output data port.

6. (Original) The serializer of claim 1 further comprising means for loading the register from a parallel bus.

7. (Original) The serializer of claim 1 wherein the pulse generator signals, that define the serially output data word bits, provide a logic transition that defines when the data word bits being sent out are stable.

8. (Original) The serializer of claim 1 wherein the pulse generator runs at twice the data bit rate wherein the data bits are shifted out on one pulse edge and the following pulse edge defines when the data word bits being sent out are stable.

9. (Original) The serializer of claim 1 further comprising;

a load signal that loads the data word bits into the register; and

a synchronizer that synchronizes the pulse generator to the load signal, so that the data word bits are stable in the register before they are output.

10. (Original) The serializer of claim 1 further comprising:

means for connecting the pulse generator output to one or more additional registers for holding additional data words; and

wherein the additional data words are delivered to one or more additional output ports and serially output in response to the pulse generator, and further wherein signals from the pulse generator are output that define the output data word bits.

11. (Original) The serializer of claim 1 further comprising:

a load signal that loads the data word bits into the register; and

means for enabling the pulse generator with the load signal, wherein the pulse generator provides a stream of pulses sufficient to output the data word after the data word bits are stable in the register.

12. (Original) The serializer of claim 1 further comprising:

means for detecting a change in the data word to be sent, and in response thereto, causing the data word bits to be output via the output data port.

13. (Previously Presented) A deserializer arranged to receive a data word bit by bit, the deserializer comprising:

a serial input port for receiving the data word bit by bit;

a register for storing the data word bits, the register having a data input and a control input;

means for connecting the serial input port to the register data input;

a pulse generator receiving port for receiving pulses that defines the data word bits;

means for connecting the received pulses to the control input, wherein the data word bits are serially received and stored in the register, and

means for detecting at least two bits added to the data word bits, wherein the added two bits always include a logic one and a logic zero in any order, and further wherein the signals on the pulse generator receiving port stay at a constant logic level during the receipt of the at least two added bits.

14. (Previously Presented) The deserializer of claim 13 further comprising means for detecting a data word boundary that separates data words, the data word boundary comprised of a combination of signals on the pulse generator receiving port and the at least two bits added to the data word bits.

15. (Canceled)

16. (Original) The deserializer of claim 13 wherein the register for storing data is a shift register.

17. (Original) The deserializer of claim 13 further comprising means for reading the register contents via a parallel port.

18. (Currently Amended) A serializer/deserializer for sending a data word out bit by bit and for receiving a data word bit by bit, the serializer/deserializer comprising:

a first register for holding the data word, the first register having at least one data output and a first control input;

an output data port for serially outputting the data word bits by bit;

means for connecting the first register at least one data output to the output data port;

a pulse generator free of external timing reference;

means for connecting the pulse generator to the first control input after a data word has been loaded into the first register, wherein the data word bits are serially output in response to the pulse generator;

means for adding at least two boundary bits to the serially output data word bits, wherein the added at least two bits always include a logic one and the logic zero in any order, and further wherein the means for connecting the pulse generator to the first control input includes means for holding the signal at the control input at a constant logic level during the outputting of the at least two added bits,;

a serial input port for receiving the data word bit by bit;

a second register for storing the data word bits, the second register having a data input and a control input;

means for connecting the serial input port to the second register data input;

a pulse generator receiving port for receiving pulses that defines the data word bits;

means for connecting the received pulses to the control input, wherein the data word bits are serially received and stored in the second register, and

means for detecting at least two bits added to the data word bits, and further wherein the signals on the pulse generator receiving port stay at a constant logic level during the receipt of the at least two added bits.

19. (Previously Presented) The serializer/deserializer of claim 18 further comprising:

means for detecting a change in the data contents of the first register, and in response thereto, causing the data word bits to be output via the output data port; and

data outputs from the second register wherein the second register contents are available.

20. (Previously Presented) A process for serializing and sending a data word out bit by bit, the process comprising the steps of:

holding the data word in a the register having at least one data output and a control input;

connecting the data output to the output data port;

generating pulses free of external timing reference;

connecting the pulse generator to the control input after a data word has been loaded into the register, wherein the data word bits are serially output bit by bit;

outputting signals from the pulse generator to define the serially output data word bits, and

adding two boundary bits to the serially output data word bits, wherein the added two bits always include a logic one and a logic zero in any order; and

maintaining the pulse generator output at a constant logic level during the outputting of the two added bits.

21-22. (Canceled)

23. (Original) The process of claim 20 wherein the register is a shift register and the step of outputting the data word bits includes shifting the data word bits out of the shift register.

24. (Original) The process of claim 20 wherein the step of outputting the data word bits includes demultiplexing the register outputs and connecting them to the output data port.

25. (Original) The process of claim 20 further comprising the step of loading the register from a parallel bus.

26. (Original) The process of claim 20 wherein the step of outputting signals from pulse generator includes the step of providing a logic transition that defines when the data word bits being sent out are stable.

27. (Original) The process of claim 20 further comprising the step of operating the pulse generator runs at twice the data bit rate wherein the data bits are shifted out on one pulse edge and the following pulse edge defines when the data word bits being sent out are stable.

28. (Original) The process of claim 20 further comprising the steps of:

loading the data word bits into the register; and

synchronizing the pulse generator to the load signal, so that the data word bits are stable in the register before they are output.

29. (Original) The process of claim 20 wherein further comprising the steps of:

connecting the pulse generator output to one or more additional registers for holding additional data words; and

wherein the additional data words are delivered to one or more additional output ports and serially output in response to the pulse generator, and further wherein signals from the pulse generator are output that define the output data word bits.

30. (Original) The process of claim 20 further comprising the steps of:

loading the data word bits into the register; and

enabling the pulse generator with the load signal, wherein the pulse generator provides a stream of pulses sufficient to output the data word after the data word bits are stable in the register.

31. (Original) The process of claim 20 further comprising the steps of:

detecting a change in the data word to be sent, and in response thereto, causing the data word bits to be output via the output data port.

32. (Previously Presented) A process for receiving and deserializing a data word bit by bit, the process comprising the steps of:

receiving the data word bit by bit via a serial input port;

connecting the serial input port to the register data input;

storing the data word bits in a register having a data input and a control input;

receiving pulses that defines the data word bits;

connecting the received pulses to the control input, wherein the data word bits are serially received and stored in the register; and

detecting two bits added to the data word bits, wherein the added two bits always include a logic one and a logic zero in any order; and

detecting signals on the pulse generator receiving port that remain at a constant logic level during the receipt of the two added bits.

33-34 (Canceled)

35. (Original) The process of claim 32 wherein the register for storing data is a shift register and the step of storing the data word includes shifting the data word bits into the shift register.

36. (Original) The process of claim 32 further comprising the step of reading the register contents via a parallel port.

37. (Previously Presented) A process for serializing and deserializing a data word sent out bit by bit and received bit by bit, the process comprising:

holding the data word in a first register having at least one data output and a control input;

connecting the data output to the output data port;

generating pulses free of external timing reference;

connecting the pulse generator to the control input after a data word has been loaded into the first register, wherein the data word bits are serially output bit by bit;

outputting signals from the pulse generator to define the serially output data word bits;

adding two boundary bits to the serially output data word bits, wherein the added two bits always include a logic one and a logic zero in any order;

maintaining the pulse generator output at a constant logic level during the outputting of the two added bits;

receiving the data word bit by bit via a serial input port;

connecting the serial input port to a second register data input;

storing the data word bits in the second register having a data input and a control input;

receiving pulses that defines the data word bits; and

connecting the received pulses to the control input, wherein the data word bits are serially received and stored in the second register; and

detecting at least two bits added to the data word bits and that the signal on the pulse generator receiving port stay at a constant logic level during the receipt of the at least two added bits.

38. (Original) The process of claim 37 further comprising the steps of:

detecting a change in the data word to be sent, and in response thereto, causing the data word bits to be output via the output data port; and

reading the second register contents via a parallel port.

39. (Original) A computer system comprising:

a processor, memory, and an input/output apparatus, wherein the input/output apparatus comprises the serializer as defined in claim 1.

40. (Canceled)

41. (Original) A computer system comprising:

a processor, memory, and an input/output apparatus, wherein the input/output apparatus comprises the deserializer as defined in claim 13.

42. (Previously Presented) A computer system comprising:

a processor, memory, and an input/output apparatus, wherein the input/output apparatus comprises the serializer/deserializer as defined in claim 18.

43. (Original) A digital camera system comprising an optical system and means for digitizing optical signals and a processor, memory, and an input/output apparatus arranged for process the digitized optical signals, wherein the input/output apparatus comprises the serializer as defined in claim 1.

44. (Canceled)

45. (Previously Presented) A digital camera system comprising an optical system and means for digitizing optical signals and a processor, memory, and an input/output apparatus arranged for process the digitized optical signals, wherein the input/output apparatus comprises the deserializer as defined in claim 13.

46. (Previously Presented) A digital camera system comprising an optical system and means for digitizing optical signals and a processor, memory, and an input/output apparatus arranged for process the digitized optical signals, wherein the input/output apparatus comprises the serializer/deserializer as defined in claim 18.

47. (Original) A digital memory system comprising:

an input/output apparatus, wherein the input/output apparatus comprises the serializer as defined in claim 1.

48. (Canceled)

49. (Previously Presented) A digital memory system comprising:

an input/output apparatus, wherein the input/output apparatus comprises the deserializer as defined in claim 13.

50. (Previously Presented) A digital memory system comprising:

an input/output apparatus, wherein the input/output apparatus comprises the serializer/deserializer as defined in claim 18.

51. (Original) A digital system having a parallel data bus comprising the serializer as defined in claim 1.

52. (Original) The digital system of claim 51 wherein the digital system is selected from the group consisting of a scanner, a keyboard, and a printer, and further comprising the serializer as defined in claim 1, or claim 11, or the serializer/deserializer defined in claim 18.